What is Claimed is:

1. Integrated circuit antifuse circuitry, comprising:

a metal-insulator-semiconductor antifuse transistor having a drain, source, gate, and substrate, wherein the drain and substrate form a drain-substrate p-n junction, wherein the substrate and source form a substrate-source p-n junction, and wherein the gate has a gate insulator; and

circuitry that applies voltages to the antifuse transistor that forward bias the substrate-source p-n junction and that cause avalanche breakdown of the drain-substrate p-n junction to produce a sufficient concentration of hot carriers to break down the gate insulator and program the antifuse.

2. The integrated circuit antifuse circuitry defined in claim 1 wherein the gate insulator comprises gate oxide.

3. The integrated circuit antifuse circuitry defined in claim 1 further comprising sensing circuitry that senses whether the antifuse transistor has been programmed and outputs a high or low logic signal accordingly.

4. The integrated circuit antifuse circuitry defined in claim 1, wherein the antifuse transistor is used on an integrated circuit having a power supply voltage, the integrated circuit antifuse circuitry further comprising a charge pump that produces a

programming supply voltage having a magnitude greater than the power supply voltage, wherein the programming supply voltage is used to program the antifuse transistor.

5. The integrated circuit antifuse circuitry defined in claim 1 further comprising a resistor connected between the substrate and the source.

6. The integrated circuit antifuse circuitry defined in claim 1 further comprising a conductor that electrically interconnects the gate and the source.

7. The integrated circuit antifuse circuitry defined in claim 1 further comprising a resistor that connects the drain to a positive power supply voltage.

8. The integrated circuit antifuse circuitry defined in claim 1 wherein the gate is electrically connected to the source, the integrated circuit antifuse circuitry further comprising:

a first resistor connected between the drain and a positive power supply voltage; and

a second resistor connected between the substrate and a ground potential.

9. The integrated circuit antifuse circuitry defined in claim 1 wherein the drain, source, and substrate are surrounded by an isolating well.

10. The integrated circuit antifuse circuitry

defined in claim 1 wherein the circuitry that applies the voltages comprises at least one Zener diode connected between the drain and substrate and at least one resistor connected between the substrate and the source, wherein the Zener diode is reverse biased and breaks down to allow current to flow from the Zener diode through the resistor to help forward bias the substrate-source p-n junction.

11. The integrated circuit antifuse circuitry defined in claim 1 wherein the circuitry that applies the voltages comprises at least one gated diode connected between the drain and substrate and at least one resistor connected between the substrate and the source, wherein the gated-diode is reverse-biased and breaks down to allow current to flow from the gated diode through the resistor to help forward bias the substrate-source p-n junction.

12. The integrated circuit antifuse circuitry defined in claim 1 wherein the circuitry that applies the voltages comprises a voltage divider circuit that applies a bias voltage to the substrate during programming of the antifuse to forward bias the substrate-source p-n junction.

13. The integrated circuit antifuse circuitry defined in claim 1 wherein the antifuse transistor is programmed during programming and is sensed during sensing and wherein the circuitry that applies the voltages comprises:

a voltage divider circuit that applies a bias voltage to the substrate during programming of the antifuse to forward bias the substrate-source p-n junction; and

a switch that prevents application of the bias voltage to the substrate during sensing.

14. The integrated circuit antifuse circuitry defined in claim 1 wherein the antifuse transistor is fabricated using a semiconductor fabrication process having a design rule that allows transistor gates to be fabricated with a particular minimum allowed gate length and wherein the gate of the antifuse transistor has an associated length that is greater than the minimum allowed gate length.

15. The integrated circuit antifuse circuitry defined in claim 1 wherein the circuitry that applies the voltages is formed on an integrated circuit having I/O circuitry powered by an I/O power supply voltage, wherein the circuitry that applies the voltages applies the I/O power supply voltage to the drain.

16. The integrated circuit antifuse circuitry defined in claim 1 wherein the gate is electrically connected to the source, the integrated circuit antifuse circuitry further comprising:

a resistor connected between the drain and a positive voltage; and

a second resistor connected between the substrate and a ground potential.

17. The integrated circuit antifuse circuitry defined in claim 1 further comprising a current limiting resistor connected to the antifuse transistor that limits how much current is applied to the antifuse transistor when the antifuse transistor is programmed.

18. The integrated circuit antifuse circuitry defined in claim 1 wherein there are at least two different doping concentrations in the substrate adjacent to the drain so that the drain-substrate p-n junction is one of at least two parallel drain-substrate p-n junctions, wherein each of the drain-substrate p-n junctions experiences reverse breakdown at a different reverse-bias voltage level.

19. The integrated circuit antifuse circuitry defined in claim 1 wherein the metal-insulator-semiconductor antifuse transistors are formed on a silicon-on-insulator substrate.

20. A method of programming an antifuse transistor that is formed from a semiconductor and that has a drain, a source, and a gate having a gate insulator, comprising:

during programming, injecting hot carriers into the substrate under the gate insulator to break down the gate insulator and program the antifuse transistor, wherein more hot carriers are injected into the substrate at the drain than at the source so that the gate insulator is stressed asymmetrically.

21. The method defined in claim 20, wherein the antifuse transistor is formed from a semiconductor and has a substrate, wherein the drain and substrate form a drain-substrate p-n junction in the semiconductor, wherein the substrate and source form a substrate-source p-n junction in the semiconductor, and wherein a resistor is connected to the substrate, the method further comprising:

flowing current through the resistor to raise the voltage of the substrate relative to the source during programming to forward bias the substrate-source p-n junction.

22. The method defined in claim 20, wherein the antifuse transistor is formed from a semiconductor and has a substrate, wherein the drain and substrate form a drain-substrate p-n junction in the semiconductor, wherein the substrate and source form a substrate-source p-n junction in the semiconductor, and wherein a resistor is connected to the substrate, the method further comprising:

flowing current through the resistor to raise the voltage of the substrate relative to the source to forward bias the substrate-source p-n junction, wherein forward biasing the substrate-source p-n junction injects carriers into the substrate, which increases current flow through the resistor that further raises the voltage of the substrate.

23. The method defined in claim 22 wherein

flowing the current through the resistor to raise the voltage of the substrate comprises using at least one reverse-biased Zener diode in breakdown to help cause current to flow through the resistor.

24. The method defined in claim 22 wherein flowing the current through the resistor to raise the voltage of the substrate comprises using at least one reverse-biased gated diode in breakdown to help cause current to flow through the resistor.

25. The method defined in claim 22 wherein a resistor is connected to the substrate, wherein there are at least two regions of the substrate adjacent to the drain that have different doping levels so that there are at least two drain-substrate p-n junctions in parallel each having a different associated reverse-bias breakdown voltage, and wherein flowing the current through the resistor to raise the voltage of the substrate comprises using the two parallel p-n junctions to cause current to flow through the resistor to raise the voltage of the substrate.

26. The method defined in claim 20, wherein the antifuse transistor is formed from a semiconductor and has a substrate, wherein the drain and substrate form a drain-substrate p-n junction in the semiconductor, and wherein the substrate and source form a substrate-source p-n junction in the semiconductor, the method further comprising:

using a switch and voltage divider

circuit to raise the voltage of the substrate relative to the source during programming to forward bias the substrate-source p-n junction.

27. The method defined in claim 20 wherein the antifuse transistor is formed on an integrated circuit having I/O circuitry powered by an I/O power supply voltage, the method comprising applying a voltage to the drain during programming at the I/O power supply voltage.

28. The method defined in claim 20 wherein the antifuse transistor is formed from a semiconductor and wherein injecting hot carriers into the substrate under the gate insulator to break down the gate insulator comprises injecting hot carriers into the substrate under the gate insulator to break down the gate insulator without melting the semiconductor.